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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,920	02/28/2002	Ronald P. Cocchi	PD-200337	1161

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THE DIRECTV GROUP INC
PATENT DOCKET ADMINISTRATION RE/R11/A109
P O BOX 956
EL SEGUNDO, CA 90245-0956

EXAMINER	
ZIA, SYED	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/085,920	COCCHI ET AL.	
	Examiner	Art Unit	
	Syed Zia	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to amendment, and request for reconsideration filed on April 13, 2007. Original application contained Claims 1-28. Applicant currently amended Claims 1, 8, 15, and 22. Applicant previously amended Claims 1, 8, 15, and 22. Applicant's amendments filed on April 13, 2007 has been entered and made of record Therefore, Claims 1-28 are pending for further consideration.

Response to Arguments

Applicant's arguments filed on April 13, 2007 have been fully considered but they are not persuasive because of the following reasons:

Regarding Claims, 1, 8, 15, and 22 applicants argued that the cited prior art (CPA) Kocher (U.S. Patent 6,289,455) does not teach or suggest that " *a microprocessor's non-protected nonvolatile memory component and the protected nonvolatile memory component use physical and logical address ranges that are the same*" .

This is not found persuasive. Cited prior art teaches a system and method that relates to cryptographic unit connected in between a microprocessor and memory for protecting the memory from microprocessor by cryptographically transforming data communicated in between microprocessor and memory. The cryptographic unit for transforming data from microprocessor uses memory contents and transformation result is utilized to decode digital content. Cryptographic right unit CRU includes an interface control processor (ICP), which is responsible

for communication with playback device via I/O interface. In addition, CRU includes several types of memory connected to interface control processor via bus. In particular, fixed data and code are stored in ROM, temporary data (and possibly code) are stored in RAM, and additional code and/or data are stored in EEPROM which can be modified by processor. Also attached to bus is CryptoFirewall, a specialized cryptographic processing unit which regulates and cryptographically modifies data written to or read from protected memory (col.9 line 29 to line 59 and (col.27 line 25 to line 39).

Kocher further teach or disclose of switching device(s) (such as programming charge pump) to control the connection of voltages to memory in a I/O environment, such as hardware architecture of Kochner (Fig.2, col.21 line 34 toline 64).

Thus the system of cited prior art provides a system and method for preventing unauthorized access to digital services.

Therefore, the examiner asserts that cited prior art does teach or suggest the subject matter recited in independent Claims 1, 8, 15, 22, and in subsequent dependent Claims. Accordingly, rejections for claims 1-28 are respectfully maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Kocher (U.S. Patent 6,289,455).

1. Regarding Claim 8 Kocher teaches a method for limiting unauthorized access to digital services comprising:

(a) configuring a protected nonvolatile memory component (col.21 line 13 to line 15), wherein: (i) the protected nonvolatile memory component is used to contain state information to provide desired functionality and enforce one or more security policies (i.e. regulating access) for accessing the digital services (col.10 line 5 to line 47, and col.5 line 55 to col.6line 3); and (ii) programming control and a programming charge pump are shared by both the protected nonvolatile memory component and a microprocessor's non-protected nonvolatile memory component; (iii) the microprocessor's non-protected nonvolatile memory component and the protected nonvolatile memory component use physical and logical address ranges that are the same (col.27 line 25 to line 39) and (b) controlling access to the nonvolatile memory component through a fixed state custom logic block, and wherein data and address lines of the protected nonvolatile memory component are routed only to the fixed state custom logic block (col. 21 line 2 to col. 22 line 25).

2. Regarding Claim 15 Kocher teaches a conditional access module (CAM), (Fig. 2 Item 225) comprising:

(a) a protected nonvolatile memory component (col.21 line 13 to line 15), wherein: (i) the protected nonvolatile memory component is used to contain state information to provide desired functionality and enforce one or more security policies (i.e. regulating access) for accessing digital services (col.10 line 5 to line 47, and col.5 line 55 to col.6line 3); and (ii) programming control and a programming charge pump are shared by both the protected nonvolatile memory component and a microprocessor's non-protected nonvolatile memory component; (iii) the microprocessor's non-protected nonvolatile memory component and the protected nonvolatile memory component use physical and logical address ranges that are the same (col.27 line 25 to line 39) ; and (b) a fixed state custom logic block configured to control access to the nonvolatile memory component, and wherein data and address lines of the protected nonvolatile memory component are routed only to the fixed state custom logic block (col. 21 line 2 to col. 22 line 25).

3. Regarding Claim 22 Kocher teaches a. An article of manufacture for preventing unauthorized access to digital services comprising:

(a) means for configuring a protected nonvolatile memory component (col.21 line 13 to line 15), wherein: (i) the protected nonvolatile memory component is used to contain state information to provide desired functionality and enforce one or more security policies (i.e. regulating access) for accessing the digital services (col.10 line 5 to line 47, and col.5 line 55 to col.6line 3); and (ii) programming control and a programming charge pump are shared by both

the protected nonvolatile memory component and a microprocessor's non-protected nonvolatile memory component; (iii) the microprocessor's non-protected nonvolatile memory component and the protected nonvolatile memory component use physical and logical address ranges that are the same (col.27 line 25 to line 39); and (b)means for controlling access to the nonvolatile memory component through fixed state custom logic block, and wherein data and address lines of the protected nonvolatile memory component are routed only to the fixed state custom logic block (col. 21 line 2 to col. 22 line 25).

4. Claims 9-14, 16-21, and 23-28 are rejected applied as above rejecting Claim 8, 15, and 22. Furthermore, Kocher teaches and describes a system and method for controlling access to digital services, wherein:

As per Claim 9, the custom logic block has a fixed algorithm that cannot be altered by external means (Kocher: col.23 line 36 to line 48).

As per Claim 10, access to a block of the protected nonvolatile memory component is limited to one or more functions defined in the custom logic block (Kocher: col.24 line 10 to line 30).

As per Claim 11, the custom logic block is implemented in solid state hardware that implements a simple and well defined state machine (Kocher: col.4 line 1 to line 13).

As per Claim 12, the protected nonvolatile memory component is not accessible through a system input/output module, system bus, microprocessor, or external environment (Kocher: col. 21 line 2 to line 64).

As per Claim 13, the nonvolatile memory component is exclusively controlled through the custom logic block and does not require the use of a system bus or microprocessor (Kocher: col.21 line 13 to line 21).

As per Claim 14, a microprocessor's nonvolatile memory component and the protected nonvolatile memory component use the same physical and logical address ranges (Kocher: col.27 line 25 to line 39).

As per Claim 16, the custom logic block has a fixed algorithm that cannot be altered by external means. (Kocher: col.23 line 36 to line 48).

As per Claim 17, access to a block of the protected nonvolatile memory component is limited to one or more functions defined in the custom logic block Kocher: col.24 line 10 to line 30).

As per Claim 18, the custom logic block is implemented in solid state hardware that implements a simple and well defined state machine (Kocher: col.4 line 1 to line 13).

As per Claim 19, the protected nonvolatile memory component is not accessible through a system input/output module, system bus, microprocessor, or external environment (Kocher: col. 21 line 2 to line 64).

As per Claim 20, the nonvolatile memory component is exclusively controlled through the custom logic block and does not require the use of a system bus or microprocessor (Kocher: col.21 line 13 to line 21).

As per Claim 21, a microprocessor's nonvolatile memory component and the protected nonvolatile memory component use the same physical and logical address ranges (Kocher: col.27 line 25 to line 39).

As per Claim 23, the custom logic block has a fixed algorithm that cannot be altered by external means (Kocher: col.23 line 36 to line 48).

As per Claim 24, access to a block of the protected nonvolatile memory component is limited to one or more functions defined in the custom logic block Kocher: col.24 line 10 to line 30).

As per Claim 25, the custom logic block is implemented in solid state hardware that implements a simple and well defined state machine (Kocher: col.4 line 1 to line 13).

As per Claim 26, the protected nonvolatile memory component is not accessible through a system input/output module, system bus, microprocessor, or external environment (Kocher: col. 21 line 2 to line 64).

As per Claim 27, the nonvolatile memory component is exclusively controlled through the custom logic block and does not require the use of a system bus or microprocessor (Kocher: col.21 line 13 to line 21).

As per Claim 28, a microprocessor's nonvolatile memory component and the protected nonvolatile memory component use the same physical and logical address ranges (Kocher: col.27 line 25 to line 39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen et al. (U. S. Patent 5,282,249), and further in view of Kocher (U.S. Patent 6,289,455).

6. Regarding Claim 1, Cohen teach and describe a system for controlling access to digital services comprising: (a) a control center configured to coordinate and provide digital services; (b) an uplink center configured to receive the digital services from the control center and transmit the digital services to a satellite (Fig. 1/1 Item 20); (c) the satellite configured to: (i) receive the digital services from the uplink center (Fig. 1/2 Item 22); (ii) process the digital services (Fig. 1/2 Item 22), and (iii) transmit the digital services to a subscriber receiver station (Fig. 1/2 Item 24); (d) the subscriber receiver station configured to: (i) receive the digital services from the satellite (Fig. 1/2 Item 26); (a) control access to the digital services through an integrated receiver/decoder IRD) (Fig. 1/2 Item 30); and (e)a conditional access module (CAM) communicatively coupled to the IRD (Fig. 1/2 Item 32), [col.4 line 12 to line 66],

Cohen do not disclose the CAM comprising nonvolatile protected memory component having state information to enforce desired functionality.

However, Kocher disclose the CAM (Fig.2 Item 225) comprising:

(i) a protected nonvolatile memory component, wherein: (1)the protected nonvolatile memory component (col.21 line 13 to line 15) is used to contain state information to provide desired functionality and enforce one or more security policies (i.e. regulating access) for accessing the digital services (col.10 line 5 to line 47,and col.5 line 55 to col.6line 3); (2) programming control

and a programming charge pump are shared by both the protected nonvolatile memory component and a microprocessor's non-protected nonvolatile memory component;

(3) the microprocessor's non-protected nonvolatile memory component and the protected nonvolatile memory component use physical and logical address ranges that are the same (col.27 line 25 to line 39); and (ii) a fixed state custom logic block configured to control access to the nonvolatile memory component, and wherein data and address lines of the protected nonvolatile memory component are routed only to the fixed state custom logic block (col. 21 line 2 to col. 22 line 25).

Kocher is analogous art because it discusses a method and apparatus for preventing piracy of digital content including the use of a smart card.

Therefore, It would have been obvious to one ordinary skilled in the art at the time of invention to include the teachings and features of CAM found in Kocher in the smart card used by Cohen, to control access to the broadcast data, because Kocher's method of protected memory of monitored data by using state information would not only promote security structure in the system of Cohen during receiving and distributing digital content (Kocher: col.5 line 55 to line 56) but will also provide safeguards against attempt by unauthorized person to breach security of system.

7. Claims 2-7 are rejected applied as above rejecting Claim 1. Furthermore, system of Cohen and Kocher teaches and describes a system and method for controlling access to digital services, wherein:

As per Claim 2, the custom logic block has a fixed algorithm that cannot be altered by external means (Kocher: col.23 line 36 to line 48).

As per Claim 3, access to a block of the protected nonvolatile memory component is limited to one or more functions defined in the custom logic block (Kocher: col.24 line 10 to line 30).

As per Claim 4, the custom logic block is implemented in solid state hardware that implements a simple and well defined state machine (Kocher: col.4 line 1 to line 13).

As per Claim 5, the protected nonvolatile memory component is not accessible through a system input/output module, system bus, microprocessor, or external environment (Kocher: col. 21 line 2 to line 64).

As per Claim 6, the nonvolatile memory component is exclusively controlled through the custom logic block and does not require the use of a system bus or microprocessor (Kocher: col.21 line 13 to line 21).

As per Claim 7, a microprocessor's nonvolatile memory component and the protected nonvolatile memory component use the same physical and logical address ranges (Kocher: col.27 line 25 to line 39).

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1, 8, 15, and 22 of instant application 10085920 (hereafter '920) are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 10, 19, and 28 of copending Application No. 10085346 (hereafter '346). Although the conflicting claims are not identical, they are not patentably distinct from each other because in view of the obviousness type double patenting rationale enunciated in **Georgia-Pacific Corp. v. United States Gypsum Co., 195 F.3d 1322, 1326, 52 USPQ2d 1590, 1593 (Fed. Cir. 1999**, the instant application's above mentioned claims merely define a system for controlling access to digital services where device (protected memory and microprocessor) share charge pump and programming control for access right management which is a obvious variation of access rights to digital services based on hidden non-modifiable identification number of the invention as claimed in copending application '346.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Zia whose telephone number is 571-272-3798. The examiner can normally be reached on 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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January 3, 2007

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sz
June 14, 2007

SYED A. ZIA 06/14/2007
PRIMARY EXAMINER